Sensitivity Analysis of ProSEDS (Propulsive Small Expendable Deployer System) Data Communication System *

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ABSTRACT

This paper discusses analytical approaches to evaluating performance of Spacecraft On-Board Computing systems, thereby ultimately achieving a reliable spacecraft data communications systems.

The sensitivity analysis approach of memory system on the ProSEDS (Propulsive Small Expendable Deployer System) [1] as a part of its data communication system will be investigated. Also, general issues and possible approaches to reliable Spacecraft On-Board Interconnection Network and Processor Array will be shown. The performance issues of a spacecraft on-board computing systems such as sensitivity, throughput, delay and reliability will be introduced and discussed.

1   Introduction

A spacecraft communication system has inherent capabilities of providing multipoint and broadcast transmission, connectivity between any two distant nodes within a wide-area coverage, quick network configuration/reconfiguration, rapid allocation of space segment capacity, and distance-insensitive cost. To realize the capabilities above mentioned, both the size and cost of the ground-station terminals have to be reduced by using reliable, high-throughput, fast and cost-effective on-board computing system which has been known to be a critical contributor to the overall performance of space mission deployment. Controlled vulnerability of mission data (measured in sensitivity), improved performance (measured in throughput and delay) and fault tolerance (measured in reliability) are some of the most important features of these systems. The

system should be thoroughly tested and diagnosed before employing a fault tolerance into the system. Testing and fault tolerance strategies should be driven by accurate performance models (i.e. throughput, delay, reliability and sensitivity) to find an optimal solution in terms of reliability and cost. The modeling and simulation tools will be integrated with a system architecture module, a testing module and a module for fault tolerance all of which interacting through a centered graphical user interface.

This paper will investigate modeling and simulation-driven sensitivity, testability and reliability analysis for Spacecraft On-Board Computing with the ProSEDS as a model spacecraft. The work precisely will address and discuss the following specific problems.

- Develop universal sensitivity models for mission data memory. The impact of spacecraft telecommunication factors on the overall mission data processing performance will be investigated and ultimately enhancing the confidence level of mission data.

- Develop universal throughput and delay models for interconnection network under investigation. The impact of testability on the overall performance will be modeled.

- Develop performance model-driven run-time concurrent testing schemes. New packet formats will be discussed for new testing and diagnosis algorithms being driven by the performance models above mentioned.

- Develop universal reliability model-driven interconnection network with fault tolerance. The redundancy strategy will be optimized based on these models that corelate to the throughput and delay.

- Develop quality model-driven run-time and adaptive processor array repair/reconfiguration schemes. Quality-driven fault tolerance strategies will be developed by using repair algorithms.

2   Spacecraft On-Board Computing (SOBC)

The SOBC system is the heart of a spacecraft data processing system and contains required components to receive and decode commands, collect, store and playback several different types of telemetry data. The SOBC telemetry and commanding processes conform to the required recommendations (i.e. Consultative Committee for Space Data System) for packet telemetry and telecommanding. The SOBC subsystems collect mission data, ACS (Attitude Control System) data, and spacecraft housekeeping data which is stored in the high density board for later transmission during a downlink opportunity. It receives ground commands from the Transponder, executes real-time commands or time-tagged command sequences. It also forwards subsystem commands to appropriate subsystems. The telemetry mission data can be collected by the SOBC system via the high speed synchronous serial interface and/or 1553 networked-bus interface. The mission telemetry data is stored in the Bulk Memory for later use. The SOBC hardware consists of three key components: Bulk Memory, High-Speed Interconnection Network, Processor Array.

2

It is anticipated that future spacecraft will have SOBC systems to improve significantly the cost effectiveness of "thin route" service, mobile and portable communications. Advantages of SOBC systems are power efficiency, routing flexibility, decoupling of the up- and downlink noise and smaller ground terminal. The design of future spacecraft payloads is particularly demanding in view of the longevity of their missions. The reliability requirements of long duration missions impose considerable constraints on the payload due to the need for redundancy and the usage of space qualified hardware down to the component level. This in turn limits considerably the types of off-the shelf components and ASICs that can be used. In this context, the rapid development of two technologies namely programmable devices, such as field programmable gate arrays (FPGAs), and multi-chip modules (MCMs) are of particular interest. The emerging MCM technology offers significantly smaller volume, lower power consumption and potentially higher reliability implementations than those based on conventional packaging and PCB technology as evidenced by representative MCM designs. The current developments in the field of programmable device technology point to rapid technological advances and increased market penetration. The drivers behind these advances are smaller geometries, larger number of signal interconnectivity layers and novel architectures. These advances increase transistor density and lower cost per gate. The availability of programmable devices with large gate counts offers the potential of designing hardware based on novel architectures and design methodologies that aim at reconfigurable implementations. Apart from the obvious possibilities of being able to update hardware with new interfaces and algorithms, there are also possibilities of exploiting reconfigurability to improve reliability and fault tolerance not only at the chip level but at the system level through the utilization of arrays of programmable devices. Such arrays could be integrated with standard space qualified processors and RAM/ROM memories on vertically stacked and jointly packaged MCMs to form reconfigurable subsystems. Such a design approach is anticipated to result in a reduction in volume, weight, and power as well as providing additional prototyping flexibility and reduced foundry costs.

In the following section, an efficient markov-chain based approach to sensitivity analysis of the Bulk Memory will be introduced. Then, the next section will discuss Modeling and Simulation-driven interconnection network testing and fault tolerance approach and Quality-driven testing of Reconfigurable MCM processor array will be discussed in Section 4. In the final section, the work will be concluded.

3   On-Board Memory

An analytical approach to evaluating the sensitivity of spacecraft data communication system can be developed to ultimately achieve a more reliable spacecraft telecommunication.

The on-board data system continuously records, stores, and transmits mission data over the telemetry system and then downlink the data to ground stations. Vulnerability of the data communication system to mission data loss, referred to as Sensitivity, should be timely and efficiently evaluated and manipulated to assure reliability of mission with given data system/telemetry system and ground stations arrangement.

In this approach, the sensitivity is to be projected to the memory system in the data system

in a centralized manner. The memory system is to be modeled as a circular queue (4 MB in this experiment) to account for its circular write and read operations through serial ports. The memory is read out to the telemetry system and downlinked to ground stations.

The memory write and read operations are supposed to be at different rates such that write is 400 (bps) and read is 11,500 (bps). The data transmission is supposed to be unidirectional without handshakings between the subsystems. Hence, write and read operations proceed without any interruptions, which may cause overwriting the memory resulting in mission data loss. Circular writing an already-written memory segment overwrites the segment if it has not been read out to transmitter and downlinked to ground stations yet.

Novel markov-chain models are being developed, in which the states of the data communication system is defined by three logical pointers to the memory, i.e. a write pointer, a valid read pointer and lastly a pointer for general reads. State transitions are governed firstly by availability of ground stations that is available from STK (Satellite Toolkit) data and then by the probabilities of write only, read only, write/read and no operation.

The model can efficiently keep track of the number of overwrites and derives a normalized sensitivity that is defined by sum of products of all the state probabilities in which the number of overwrites is more than 0 and its corresponding ratio of overwrites, i.e. (# overwrites)/(# writes).

This approach enables us to evaluate and predict the sensitivity and will allow us to optimize cost and reliability of spacecraft communication system and its subsystems.

4   On-Board Interconnection Network

A modeling and simulation-driven testing and fault tolerance methods for on-board interconnection network can be investigated.

The model is to incorporate concurrent fault detection process to simulate the testing process as basis for a design of fault tolerant interconnection networks. The testing process is to be applicable to interconnection networks which utilize packet switching for operation in a distributed system.

A new packet format can be developed and the model is to be governed by its packet processing. Using this format, it is possible to detect in a decentralized manner the occurrence of a single fault (either in the switching mode under an unrestricted combinatorial fault model, or a stuck-at fault in either a link or a register of the switching element or the received data). This can be accomplished by comparing the subfields of the packets received at the two inputs of a switching element through the dedicated hardware, while switching is implemented in each element of the interconnection network.

The model is to be based on the new architecture of switching element for concurrent fault detection and a communication protocol. It is to be shown that detection is accomplished by at least one switching element located in the stage following the occurrence of the fault through the proposed communication protocol. Measures for concurrent fault detection such as hardware and message overheads, are also to be analyzed. The analysis is to be extended to the fault location and fault secure operation. It is to be shown that the proposed approach can accomplish these

objectives at a lower overhead and with a shorter fault latency than previous approaches. Hence, novel throughput and delay models are to be developed for new fault tolerant on-board interconnection network architecture with full link redundancy and with which various link redundancy architectures on the interconnection network for various purposes will be explored. Eventually, a new accurate and extendible reliability model is to be developed to evaluate various kinds of on-board interconnection network by using queueing model technique as a function of testing and fault tolerance factors.

5 On-Board Processors

The quality-effectiveness of the utilization of redundancy in on-board processors that can be implemented on Reconfigurable MCM (Multichip Module).

Due to the reconfigurability, Reconfigurable MCM can implement a device with different redundancy. Redundancy is determined by the requirement of the fault-tolerance of the device under implementation which is achieved by the feature of reconfigurability.

No previous work has shown the effect of utilization of redundancy on quality-level. In this work, the tolerance to escaping from testing is introduced and referred to as Escape Tolerance. This can be achieved by utilizing a certain amount of redundancy and is studied by evaluating its effect on quality level of reconfigurable MCM under different amount of redundancy. Also, it can be shown that the coverage of testing is improved by reconfiguration through numerical analysis. Hence, we derive the quality level by relating it to the reliability enhancement by reconfiguration; the effect of interconnection reliability; the effect of escape tolerance on quality level; and the improvement in fault coverage by reconfiguration.

In this approach, appropriate combinatorial models can be formulated to take into account parameters related to the redundancy and reconfiguration processes in reconfigurable MCM processors. From extensive parametric results, it can be shown that there may exist a bound in the effectiveness of redundant utilization (i.e. the amount of redundancy) depending on the value of the reconfigurable MCM reliability and fault coverage.

Using this approach, redundant utilization of reconfigurable MCM processors can be appropriately used to enhance the quality level.

6 Conclusion and Discussions

This work will establish a foundation for reliable Spacecraft On-Board Computing by developing accurate and efficient performance modeling and simulation-driven testing and fault tolerance methods and environments and thereby ultimately optimizing the cost and reliability of Spacecraft on-board data processing and telecommunication.

The performance of memory is to be modeled and simulated in terms of its sensitivity to various spacecraft telecommunication environment factors such as different ground station arrangements and involvement of relay spacecrafts. Furthermore, new ad-hoc memory operations such as writes and reads will be explored by using the performance models discussed.

The interconnection network for memory and processor modules will be tested and fault tolerated driven by the throughput and delay models and simulation tools, thereby ultimately enhancing the reliability. New interconnection network architectures will also be sought and developed driven by the modeling and simulation methods and tools discussed.

Having the optimized memory and interconnection network modules on-board, the quality of on-board processor module will be enhanced and optimized by testing and tolerating faulty processors driven by the quality models and simulation tools discussed.

Each of the three modeling and simulation modules, i.e. memory, interconnection network and processors, and its testing and fault tolerance tools will be interacting through a centered graphical user interface and monitored and controlled by an end-user.

References

[1] Systems Analysis and Integration Laboratory, Systems Engineering Division, Systems Definition & Integration Branch "Propulsive Small EXPENDABLE DEPLOYER SYSTEM (ProSEDS)", INSTRUMENTATION PROGRAM & COMMAND LIST (IP & CL), MSFC-DOC-2939, Marshall Space Flight Center, NASA, Huntsville, AL Mar.20, 1999